400G QSFP-DD LR4 Transceiver

PRODUCT FEATURES

- Compliant with 400GBASE-FR4
- 8x53.125 Gbps (PAM4) electrical interface
- Integrated CWDM EML TOSA / PIN ROSA for up to 10km reach over SMF
- Digital Diagnostics Monitoring Interface
- Duplex LC optical receptacle
- No external reference clock
- Electrically hot-pluggable
- Compliant with QSFP-DD MSA with LC connector
- Case operating temperature range:0°C to 70°C
- Power dissipation less than 12W

STANDARD

- Compliant with QSFP-DD Hardware Specification Rev 5.1
- Compliant to QSFP-DD MSA

General Description

This Multi-Source Agreement (MSA) defines 4 x 100 Gbps Coarse Wavelength Division Multiplex (CWDM) optical interface for 400 Gbps optical transceivers for Ethernet applications. Forward error correction (FEC) is required to be implemented by the host in order to ensure reliable system operation. Two transceivers communicate over single mode fibers (SMF) of length from 2 meters to at least 10 kilometers. The transceiver electrical interface is eight lanes in each direction with a nominal signaling rate of 53.125 Gbps per lane.

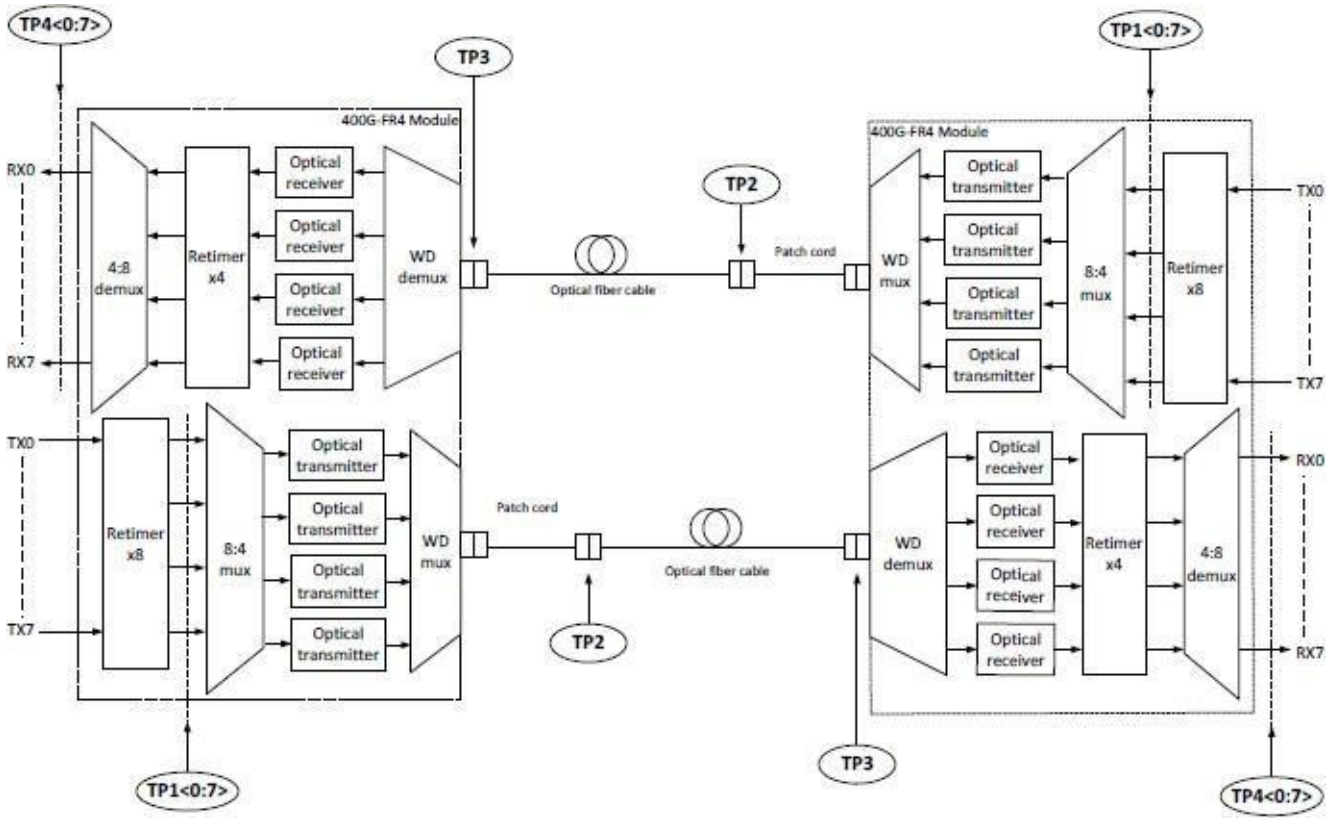


Figure 1. Block diagram for 400G-FR4 transmit/receive paths

I Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	ºC	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.5	-	3.6	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	

II Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcase	0	-	70	ºC	Without air flow
Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Power Supply Current	ICC	-		3458	mA	
Data Rate	BR		53.125		GBd	Each channel-Optical
Transmission Distance	TD		-	10	km	
Coupled fiber	Single mode fiber					9/125um SMF

III Optical Characteristics

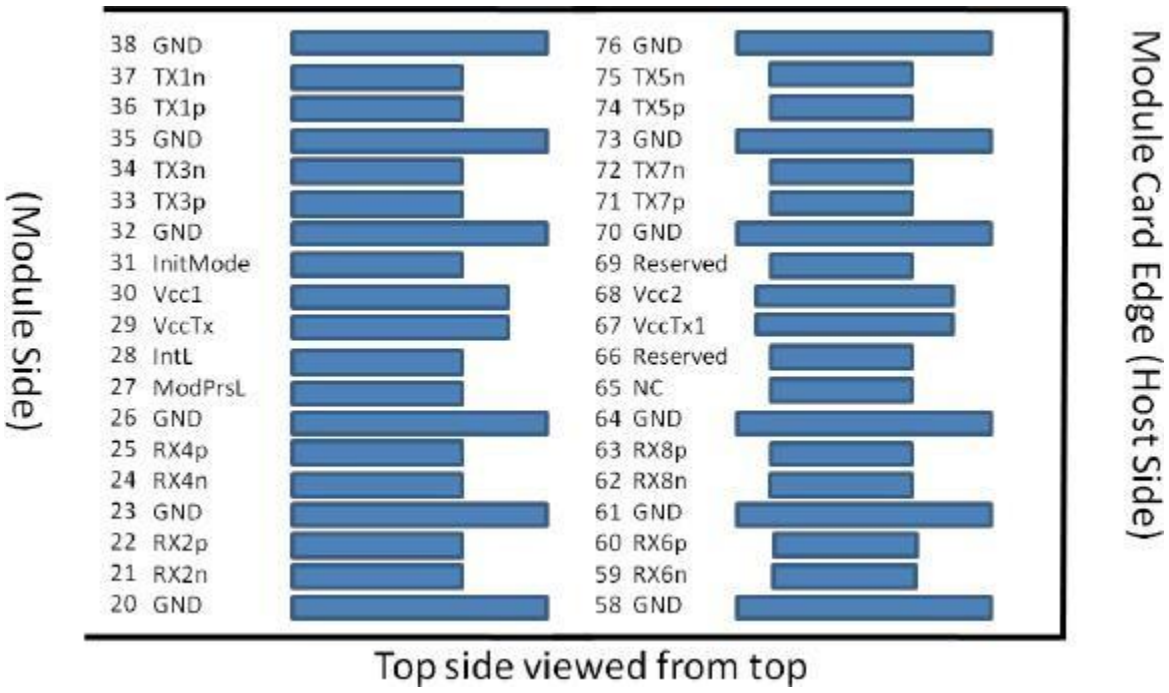
Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Transmitter						
Signaling Speed per Lane			53.125 ± 100 ppm		GBd	
Modulation format			PAM4			
Data rate variation		-100		100	ppm	
Wavelength Assignment	λ0	1264.5		1277.5	nm	
	λ1	1284.5		1297.5	nm	
	λ2	1304.5		1317.5	nm	
	λ3	1324.5		1337.5	nm	
Total Output. Power	POUT			9.3	dBm	
Transmit OMA per Lane		0.3		4.4	dBm	
Average Launch Power Per lane		-2.7		5.1	dBm	
Transmitter and Dispersion eye closure for PAM4(TDECQ) each lane	TDECQ			3.4	dB	

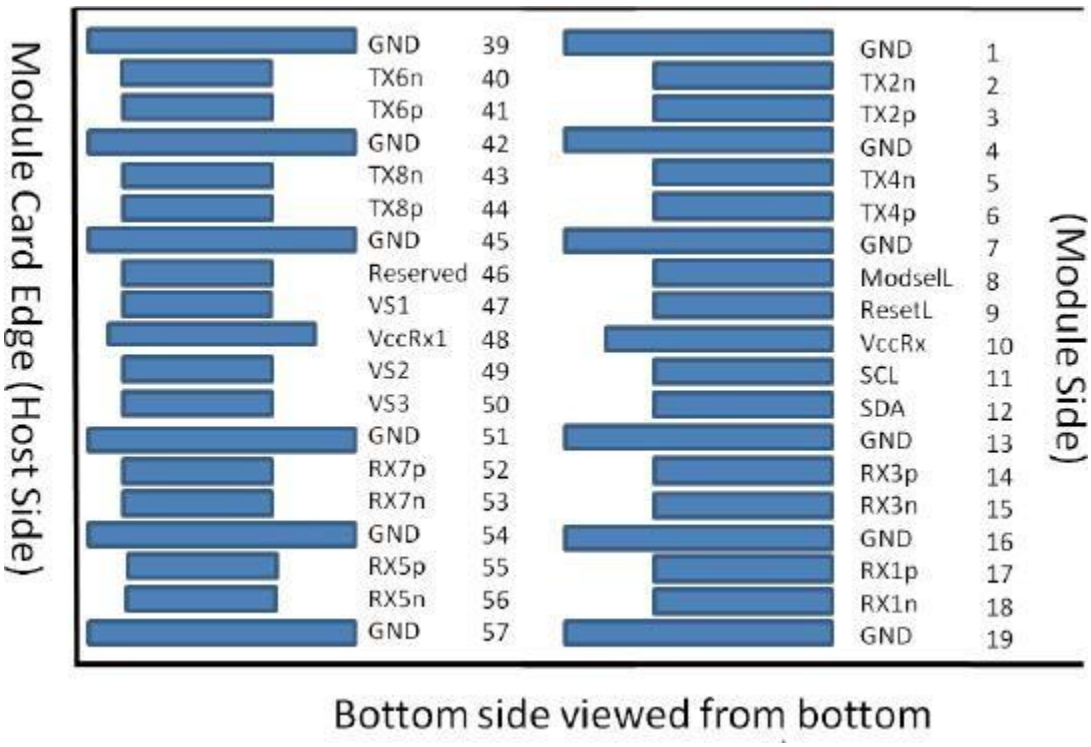
SMSR		30			dB	

Optical Extinction Ratio	ER	3.5			dB	
Average launch Power off per lane	Poff			-30	dBm	
RIN17.1OMA (max)	RIN			-136	dB/Hz	
Receiver						
Signaling Speed per Lane			53.125 ± 100 ppm		Gbps	
Modulation format			PAM4			
Data rate variation		-100		100	ppm	
Wavelength Assignment		1264.5		1277.5	nm	
		1284.5		1297.5	nm	
		1304.5		1317.5	nm	
		1324.5		1337.5	nm	
Receive Power (OMA) per Lane	ROMA			4.4	dBm	
Average Input Power per Channel	RXPx	-9		5.1	dBm	
Receiver Sensitivity (OMA) per Lane max	Rxsens			-6.8	dBm	BER@2.4E-4
Receiver Reflectance	Rr			-26	dB	

V. Pin Assignment

Figure2---Pin out of Connector Block on Host Board





Pin	Symbol	Name/Description	NOTE
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsl	Module Present	

28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For future use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	1
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For future use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

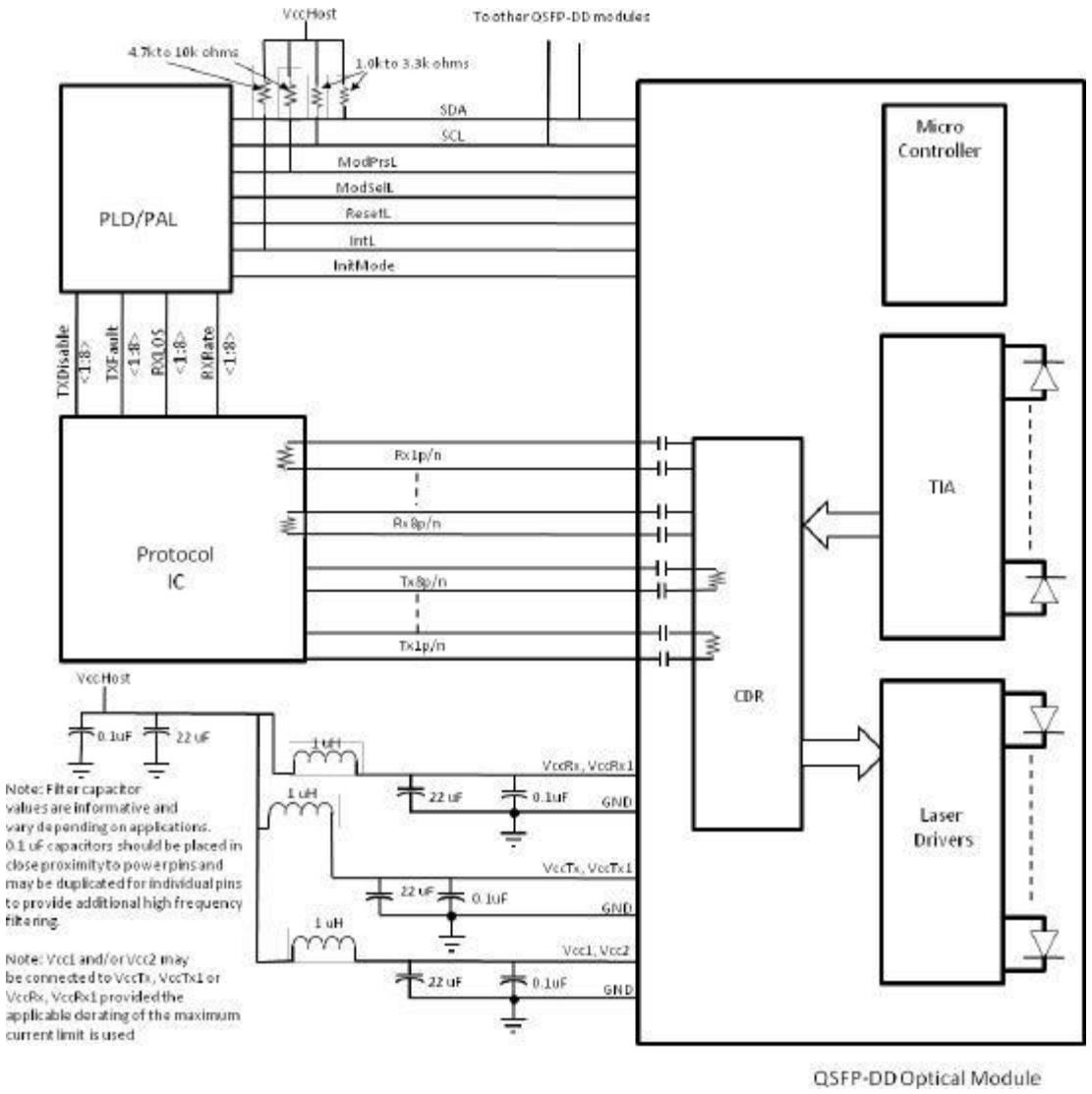
Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF .

V. Host - Transceiver Interface Block Diagram



Appendix A. Document Revision

Version No.	Date	Description
1.0	2020-09-03	Preliminary datasheet
2.0	2023-04-17	Update company logo